Taking advantage of ARM Coresight: hardware tracing in LTTng

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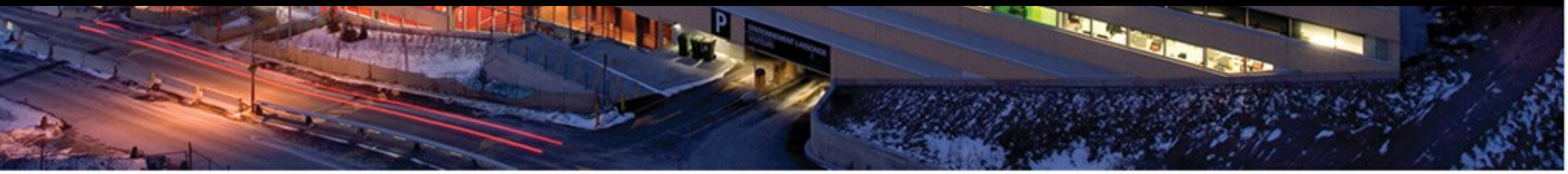


ARM Coresight

- **What is it?**
  - Collection of hardware components
  - Goal: trace and debug an entire SoC
  - Open architecture
- **Hardware tracing**
  - Very detailed info
  - Lowest overhead
  - Customizable

ARM Coresight

- **Trace sources:**
  - **Processing elements (CPU, DSP...)**
    - Can be given instruction/data IP blocks to generate trace
  - **Buses**
  - **System trace**
    - From software
- **Two main trace generators:**
  - **Embedded Trace Macrocell (ETM)**
  - **System Trace Macrocell (STM)**

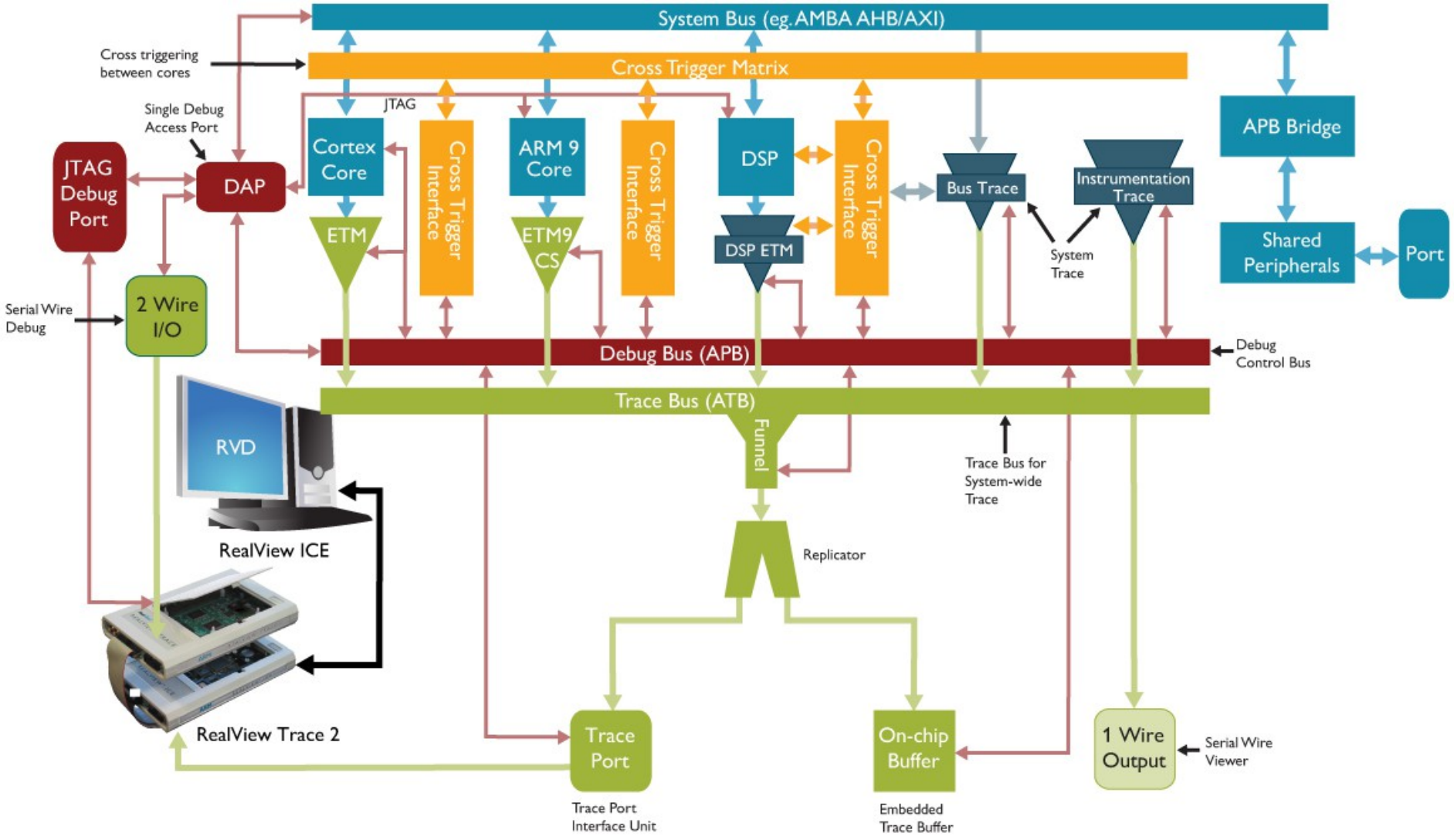
Coresight ETM

- **The Embedded Trace Macrocell (ETM)**
  - **Monitors the core's internal buses**
  - **Info on processor activity**
    - program + data
  - **No burden on performance**
  - **Data compression**
    - Full program trace ≈ 1 bit / CPU cycle
  - **Filters to capture only what wanted**

Coresight STM

- **The System Trace Macrocell (STM)**
  - **Collects info**
    - Hardware events (e.g. from bus)
    - Software (mem-mapped stimuli)
  - **Timestamps everything for correlation**
  - **Packages it and send to the trace buffer**
    - Multisource trace in a single stream
      - Optimized bandwidth
  - **Connects to the AXI system main bus**
    - Flexible
    - High-bandwidth, low latency

ARM Coresight

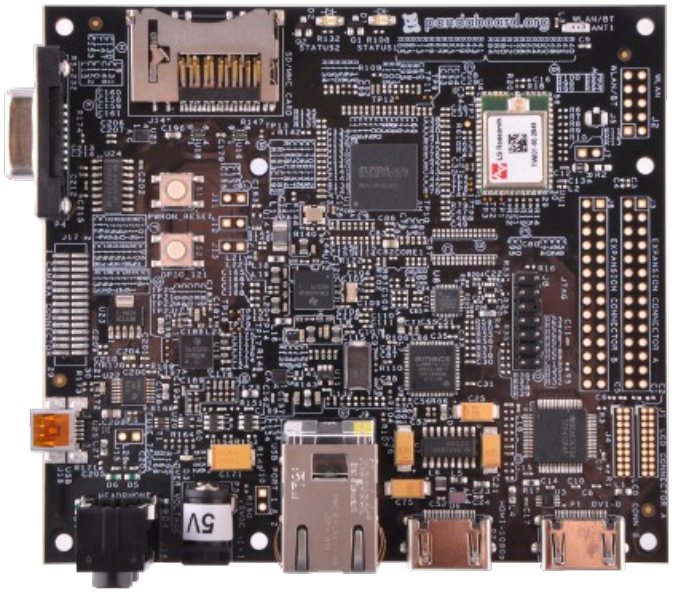


ARM Coresight

- **Standard hardware debug and trace technology**
- **Adopted by major OEMs and SiPs**
  - **NVIDIA (Tegra-2)**
  - **Texas Instrument (OMAP4)**
  - **ST-Ericsson (U8500)**
  - **Samsung (S5PCx10)**

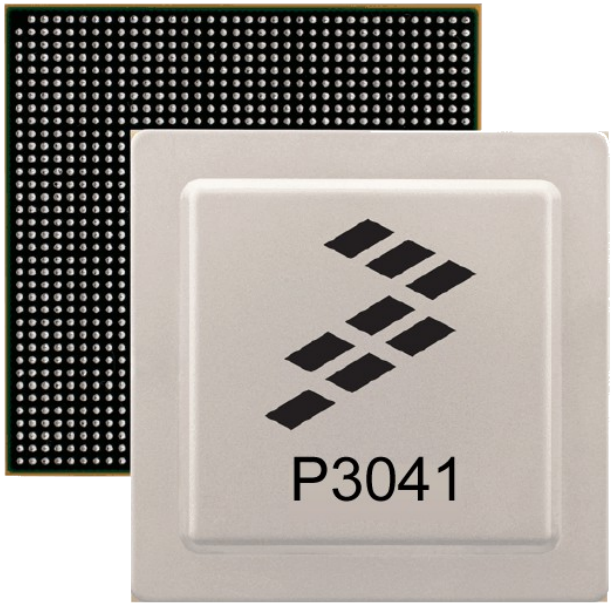
Current platform

- **Pandaboard**
  - OMAP4430 processor
  - Dual-core ARM Cortex-A9
  - ARM Coresight
  - JTAG connector



Future platform

- **Freescale QorIQ P3041**
  - **4 e500mc cores**
  - **PowerPC architecture**
  - **Performance Monitor system: can count dozens of events**
    - Processor clocks
    - Cache misses
    - Type of instructions decoded
    - Mispredicted branches



Planned work

- **Enable hardware tracing**
  - **on ARM processors**
  - **on Freescale processors**
- **Gather common characteristics**
  - **Reorganise LTTng hardware tracing architecture**
  - **Make modules for specific parts**

Thank you!

Questions?